ABSTRACT

A processing system for accessing first and second data types. The first data type is data supplied from a peripheral and the second data type is randomly accessible data held in a data memory. The processing system includes a processor for executing instructions; a stream register unit connected to supply data from the peripheral to the processor; a FIFO connected to receive data from the peripheral and connected to the stream register unit by a communication path, along which the said data can be supplied from the FIFO to the stream register unit; and a memory bus connected between the data memory and the processor, across which the processor can access the randomly accessible data.